IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF TEXAS
DALLAS DIVISION

FAST MEMORY ERASE, LLC,	§	
	§	
Plaintiff,	§	
	§	
v.	§	No. 3:08-cv-977-M
	§	
	§	
SPANSION, INC., SPANSION LLC,	§	
INTEL CORPORATION,	§	
NUMONYX B.V.,	§	
NUMONYX, INC.,	§	
STMICROELECTRONICS NV,	§	
STMICROELECTRONICS, INC.,	§	
NOKIA CORPORATION,	§	
NOKIA INC.,	§	
SONY ERICSSON MOBILE	§	
COMMUNICATIONS AB,	§	
SONY ERICSSON MOBILE	§	
COMMUNICATIONS (USA), INC.,	§	
MOTOROLA, INC. and APPLE, INC.,	§	
	§	
Defendants.	§	

FAST MEMORY ERASE, LLC,	§	
	§	
Plaintiff,	§	
	§	
v.	§	No. 3:09-cv-653-M
	§	
	§	
SPANSION, INC. and SPANSION LLC,	§	
	§	
Defendants.	§	

MEMORANDUM OPINION AND ORDER

After considering the submissions and arguments of counsel, the Court issues this Opinion and Order concerning claim construction issues.

I. Introduction

Plaintiff Fast Memory Erase, LLC filed its complaint on June 9, 2008, alleging infringement of claims 1 and 16 of U.S. patent No. 6,236,608 ("the '608 patent") and claim 1 of U.S. patent No. 6,303,959 ("the '959 patent"). The patents in issue teach a method for erasing memory cells in a semiconductor device. The Court held a *Markman* hearing on September 16, 2009. The '608 patent is being reexamined in the Patent and Trademark Office ("the PTO"). Because claims 1 and 16 of the '608 patent are subject to amendment in the PTO, this Order does not construe the '608 patent.

II. Background of the Technology

The '959 patent is directed toward reducing source leakage, which occurs during the erasure of a semiconductor device. Fast Memory asserts that the '959 patent is not limited to a particular type of semiconductor device, but is most effective in erasing non-volatile flash memory devices.

Flash memory is a technology used in memory cards and USB drives, for the storage and transfer of data between computers and other digital products. Flash memory is also widely used in mobile phones, laptops, digital audio players, and digital cameras. Since flash memory is non-volatile, no power is needed to maintain the information stored on the memory chip. Flash memory can be electronically programmed and erased, making it useful in products in which files are frequently deleted or changed.

There are four general methods for the erasure of flash memory: source erase, channel erase, gate erase, and drain erase. A central dispute in this case is whether the methods described in the '959 patent are limited to source erase or whether they are applicable to other erase procedures.

Source diode leakage, often referred to simply as source leakage, occurs during the erasure of flash memory. Source leakage lengthens erase time and degrades performance of the drive. Source leakage places a significant demand on the charge pump capacitor, the current from which is necessary to erase the device. As the source region of a semiconductor device is created, through the self-aligned source ("SAS") etch process, the etching causes a gouge and ragged edges in the source, under the edge of the stacked gate. This damage increases source leakage during erase.

The '959 patent describes a doped source region that contains at least a "first" and a "second" doped region. The second doped region has a higher concentration of dopant than the first doped region, which enhances erasure by redirecting current away from the damaged area of the source, thereby reducing source leakage.

The '959 patent is further described in the abstract:

> In one aspect, the current invention provides a method for reducing the source leakage of a semiconductor device. The method comprises the steps of stacked gate etch, thin oxide formation, SAS etch, spacer formation and source implant on the semiconductor substrate.
>
> In a second aspect, the current invention provides another method for reducing the source leakage of a semiconductor device. The method comprises the steps of stacked gate etch, first oxide layer formation, first source implant, annealing, SAS etch, second oxide layer formation, spacer formation, and second source implant.
>
> In yet another aspect, the current invention provides a novel semiconductor device. The semiconductor device is comprised of a stacked gate provided on a portion of a semiconductor substrate, a first oxide layer appended to the stacked gate, a second oxide layer formed on the first oxide layer and a spacer formed on the second oxide layer. The semiconductor device also has a doped source region having a first doped region disposed under the edge of the stacked gate and a second doped region disposed at the edge of the doped source region under the stacked gate. The second doped region has a higher concentration of dopant than the first doped region, which reduces source leakage of the semiconductor device.[1]

The disputed terms and phrases appear in Claim 1, which reads as follows:

[1] '959 Patent, at Abstract.

> 1. A semiconductor device comprising:
>
> a stacked gate provided on a portion of a semiconductor substrate;
>
> a first oxide layer provided on the edge of the stacked gate;
>
> a spacer provided adjacent the first oxide layer; and
>
> a doped source region, the source region having a first doped region disposed under the edge of the stacked gate and a second doped region disposed at the edge of the doped source region under the stacked gate;
>
> wherein the second doped region has a higher concentration of dopant than the first doped region, whereby source leakage of the semiconductor device is reduced.[2]

III. Claim Construction Standard

Claims are construed by the Court as a matter of law.[3] It is a fundamental notion of patent law that "the claims of a patent define the invention to which the patentee is entitled the right to exclude."[4] A claim term is to be given the ordinary and customary meaning that would be attributed to it by one of ordinary skill in the art at the time of the invention, which is the effective filing date of the patent application.[5] "[T]he person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification."[6]

While the Court must be guided by several principles, there is no "magic formula or catechism for conducting claim construction."[7] Publicly available sources, such as intrinsic evidence, the words of the claims, the specification, and the prosecution history, show what a person of skill in the art would have understood a disputed claim term to mean.[8] In appropriate

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[2] '959 Patent, at Cl. 1. The terms to be construed are underlined.
[3] *See Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 970-71 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996).
[4] *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)).
[5] *See Phillips*, 415 F.3d at 1313.
[6] *Id.*
[7] *Id.* at 1324.
[8] *Id.* at 1314 (quoting *Innova*, 381 F.3d at 1116).

cases, extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises, may be considered, but extrinsic evidence cannot be used to contradict the meaning of claims that are unambiguous in light of the intrinsic evidence.[9]

The *Phillips* decision emphasized the importance of the specification in claim construction.[10] The specification, of which the claims are a part, is "the single best guide to the meaning of a disputed term,"[11] since the statutory role of the specification is to describe the claimed invention in "full, clear, concise, and exact terms."[12] Nevertheless, the Federal Circuit has cautioned against importing limitations from the rest of the specification into the claims, especially when the asserted limitation derives from the description of a preferred embodiment.[13] The manner and context in which a patentee uses a term within the specification will usually make clear whether an embodiment is merely an example of the invention or whether the embodiment and claims are strictly coextensive.[14] In other words, the Court must determine "whether the specification refers to a limitation only as a part of less than all possible embodiments or whether the specification read as a whole suggests that the very character of the invention requires the limitation be a part of every embodiment."[15]

Prosecution history is part of the intrinsic record and consists of the complete record of the proceedings before the PTO, providing evidence of how the inventor and PTO understood

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[9] *Id.* at 1314, 1317. *See also C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004); *Markman*, 52 F.3d at 980 (noting that extrinsic evidence "consists of all evidence external to the patent and prosecution history . . . ."); *Galderma Labs, L.P. v. Actavis Mid-Atlantic, L.L.C.*, No. 4:06-CV-471-Y, 2008 WL 3930027, at *2 (N.D. Tex. Aug. 27, 2008).
[10] *Id*. at 1315.
[11] *Id*. (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).
[12] *Id.* at 1316 (quoting 35 U.S.C. § 112, para. 1).
[13] *Id*. at 1323. *See also Kara Tech. Inc. v. Stamps.com Inc.*, 582 F.3d 1341, 1348 (Fed. Cir. 2009).
[14] *Id*. *See also Innova*, 381 F.3d at 1117 ("[P]articular embodiments appearing in the written description will not be used to limit claim language that has broader effect. And, even where a patent describes only a single embodiment, claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction.") (citations and internal quotation marks omitted).
[15] *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1370 (Fed. Cir. 2003).

the patent.[16] The prosecution history may indicate that the inventor narrowed the scope of a claim during prosecution.[17]

Expert testimony may be helpful when providing background, explaining how an invention works, ensuring consistency with the interpretations of those skilled in the art, and establishing that a particular term has a specific meaning in the field.[18] The court will discount expert testimony that contradicts the claims, specification, and prosecution history.[19]

IV. Agreed Constructions

The parties agree to the following constructions:

(1) "provided on the edge of the stacked gate" means "provided on the side edge of the stacked gate"; and

(2) "a spacer provided adjacent the first oxide layer" means "a material provided adjacent to the first oxide layer."

The parties further agree that the Court need not construe "a doped source region."

IV. Disputed Terms to be Construed

Claim Language	**Fast Memory's Proposed Construction**	**Defendants' Proposed Construction**
"source leakage" ("whereby source leakage of the semiconductor device is reduced")	This phrase does not require construction. In the alternative only, construe as: "an unwanted and slow escape or entrance of particles or material which may be conveyed between the source terminal and ground or other parts"	leakage from the source terminal to the substrate terminal that occurs during source erase

Defendants argue that the '959 patent is limited by its specification to source erase. Plaintiff Fast Memory contends that source leakage occurs during multiple erase procedures,

[16] *See Phillips*, 415 F.3d at 1317.
[17] *Id.*
[18] *Id.* at 1318.
[19] *Id.*

including channel erase, and that the reference to a reduction of source leakage covers all such procedures.

Fast Memory argues that the term "source leakage" should not be construed, since it appears in a "whereby" clause, which generally states the result of a patented process.[20] However, when a term in a whereby clause "states a condition that is material to patentability, it cannot be ignored in order to change the substance of the invention."[21] Such an issue must be decided on the particular facts of the case.[22] A court may find that words in a whereby clause limit the claim when it "is more than the intended result of a process step; it is part of the process itself."[23] The words in a whereby clause are analyzed in light of the specification and prosecution history.[24]

The Court will construe "source leakage," because the reduction of source leakage was material to patentability. In addition to its presence in the "whereby" clause, reduced source leakage is referenced in the title,[25] abstract,[26] field of invention,[27] discussion of related art,[28]

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[20] *See Texas Instruments, Inc. v. United States Int'l Trade Comm'n*, 988 F.2d 1165, 1172, 1175 (Fed. Cir. 1993) (holding that a "whereby" clause was not limiting when it only expressed the necessary result of what was recited elsewhere in the claims); *see also Lockheed Martin Corp. v. Space Systems/Loral, Inc.*, 324 F.3d 1308, 1319 (Fed. Cir. 2003) ("a whereby clause that merely states the result of the limitations in the claim adds nothing to the substance of the claim.").

[21] *Hoffer v. Microsoft Corp.*, 405 F.3d 1326, 1329 (Fed. Cir. 2005).

[22] *See Intergraph Hardware Tech. Co. v. Toshiba Corp.*, 508 F. Supp. 2d 752, 768-69 (N.D. Cal. 2007) (citing *Griffin v. Bertina*, 285 F.3d 1029, 1034 (Fed. Cir. 2002)).

[23] *Hoffer*, 405 F.3d at 1330; *see, e.g., Lonestar Inventions LP v. Nintendo of America, Inc.*, No. 6:07-CV-261, 2009 WL 1011734, slip op. at *9 (E.D. Tex. Apr. 14, 2009) ("Although 'said first and second nodes form two opposing nodes' appears in a 'whereby clause,' the term requires construction because nowhere else in claim 1 is there a requirement to form 'opposing nodes' other than in the whereby clause. Thus, 'opposing nodes' adds a meaningful limitation to claim 1 rather than only stating an intended result.").

[24] *See id.*

[25] '959 Patent, at Title ("Semiconductor device having reduced source leakage during source erase").

[26] '959 Patent, at Abstract ("In one aspect, the current invention provides a method for reducing the source leakage of a semiconductor device.").

[27] '959 Patent 1:2-9 ("More particularly, the current invention relates to *reducing leakage* during *source erase* of flash EPROM cells. More specifically, the present invention provides new process techniques that *reduce source leakage* during source erase of flash EPROM cells. The current invention also provides novel semiconductor devices with a differentially doped source region that *reduces leakage* during *source erase*.") (emphasis added).

[28] '959 Patent 2:2-3 ("Source diode leakage must be minimized to increase source erase speed.").

summary of the invention,[29] and preferred embodiments.[30] Reduction of source leakage is integral to the invention, is part of the process itself, and was material to patentability. Thus, this term requires construction.

Defendants urge that the reference to "source leakage" in Claim 1 should be construed to refer only to leakage from the source to the substrate that occurs during source erase. Plaintiff broadly defines "source leakage" to encompass leakage during source erase, channel erase, drain erase, and gate erase. As a preliminary matter, the Court must address a disputed technical issue—whether source leakage occurs only during source erase, or whether there is also source leakage during other erasure procedures.

The '959 specification discusses source leakage in the context of source erase, and does not refer to source leakage during channel or other erase procedures.[31] However, the specification does not disclaim the possibility of source leakage during channel or other erase procedures. Fast Memory offers evidence from its expert, Dr. Liu, whose published article shows that source leakage occurs during channel erase, though there is less band-to-band tunneling than in source erase.[32] In deposition, Dr. Liu states that source leakage can travel from the source to other parts of the semiconductor device, such as the drain.[33] In response, Defendants cite the declarations of their experts, Drs. Brown and Taylor. Dr. Brown concludes that "[t]here is no source diode leakage problem or current leakage problem in channel erase . . . particularly those that float the source and drain . . . ."[34] Dr. Taylor opines that source leakage

[29] '959 Patent 3:27-28 ("The present invention addresses this need by providing new process methods that minimize source diode leakage."); 4:13-16 ("The second doped region has a higher concentration of dopant than the first doped region, which reduces source leakage of the semiconductor device.").
[30] '959 Patent 7:40-42 ("The culmative [apparently meaning cumulative] effect of these aforementioned advantages is to provide a semiconductor device with reduced levels of leakage during source erase."); 9:29-30 ("These aforementioned advantages provide a semiconductor device with reduced levels of leakage during source erase.")
[31] '959 Patent 1:66-2:3.
[32] Vei-Han Chan & David K.Y. Liu, *An Enhanced Erase Mechanism During Channel Fowler-Nordheim Tunneling in Flash EPROM Memory Devices*, 20 IEEE Electron Device Letters 140-42 (Mar. 1999).
[33] Pl.'s App. at 500 (Liu Dep. 31:22-32:9).
[34] D's App. at 250 (Brown Decl. ¶¶ 19-21).

does not occur during channel erase, because no voltage is applied to the source terminal, and the source is left floating.[35] Thus, the parties' experts disagree on this important issue. The Court is persuaded by Dr. Liu's peer-reviewed work, which was published in a respected technical journal, prior to this litigation, in which he concludes that source leakage can occur during other erase procedures.[36] Defendants produced no published works contradicting Dr. Liu's conclusions.

Although source leakage during channel erase is seemingly possible, that does not end the inquiry. The claims of a patent cannot be "of broader scope than the invention that is set forth in the specification."[37] Fast Memory's proposed construction of source leakage to include "an unwanted and slow escape or entrance of particles or material to ground or other parts" is not found in or supported by the intrinsic record. The specification states that source leakage is to the substrate during erasure, without mentioning the ground or other parts.[38] While Defendants cite no fewer than six statements in the specification describing the invention as limiting leakage during source erase,[39] Plaintiff Fast Memory points to no language in the specification which discusses the benefits of the patent in other erase procedures. In fact, the patent distinguishes

[35] D's App. at 432-33 (Taylor Decl. ¶¶ 53, 59).
[36] *See, e.g., Daubert v. Merrell Dow Pharm., Inc*., 509 U.S. 579, 593-94 (1993) ("[S]ubmission to the scrutiny of the scientific community is a component of 'good science,' in part because it increases the likelihood that substantive flaws in methodology will be detected.").
[37] *On Demand Machine Corp. v. Ingram Indus., Inc.*, 442 F.3d 1331, 1340 (Fed. Cir. 2006) (limiting a claim to the patent's specification despite a "comprising" term); *see also Alloc*, 342 F.3d at 1370 ("[W]here the specification makes clear at various points that the claimed invention is narrower than the claim language might imply, it is entirely permissible and proper to limit the claims.").
[38] '959 Patent 1:66-2:1.
[39] '959 Patent 1:2-4 ("More particularly, the current invention relates to reducing leakage during source erase of flash EPROM cells."); 1:4-6 ("More specifically, the present invention provides new process techniques that reduce source leakage during source erase of flash EPROM cells."); 1:6-9 ("The current invention also provides novel semiconductor devices with a differentially doped source region that reduces leakage during source erase."); 2:17-20 ("Thus, the difficulties caused by band to band leakage in generating and maintaining the voltage required to erase the device are frequently the limiting factor in source erasing flash cell."); 7:40-42 ("The culmative [apparently meaning cumulative] effect of these aforementioned advantages is to provide a semiconductor device with reduced levels of leakage during source erase."); 9:29-30 ("These aforementioned advantages provide a semiconductor device with reduced levels of leakage during source erase.").

channel erase as a "different method" from source erase,[40] and the specification critiques channel erase for requiring source isolation by the triple well process, which is complicated and expensive.[41] In contrast, the specification extols the benefits of source erase, which is "simpler and less expensive to implement than channel erase."[42] All of the embodiments apply to source erase.[43] The specification addresses the problem of leakage to the substrate, not to other parts of the cell.[44] The sole support in the specification for Plaintiff's broader interpretation is a reference to "alternative ways of implementing both the process and apparatus of the present invention."[45] An analysis of that statement in context reveals that the inventor was referring to dopant concentrations, not to the patent's applicability to channel erase. As noted in *Praxair*, the "claims of the patent must be read in light of the specification's consistent emphasis on [the] fundamental feature of the invention."[46]

Citing *Epistar*, Fast Memory argues that Defendants' proposed construction would impermissibly limit the '959 patent to one of its preferred embodiments.[47] However, source erase is not merely a preferred embodiment; analysis of the specification leads to the "inescapable conclusion" that the claims address only source erase.[48] In contrast to *Epistar*, support for limiting the disputed term is found throughout the specification, and the reduction of

[40] '959 Patent 1:50-51.
[41] '959 Patent 1:56-58. *See, e.g., Edward Lifesciences LLC v. Cook Inc.*, 582 F.3d 1332, 1332-33 (Fed. Cir. 2009) (limiting a claim to its specification, where the inventor disparaged prior art in the "background art" section of the specification); *see generally Astrazeneca AB v. Mut. Pharm. Co.*, 384 F.3d 1333, 1340 (Fed. Cir. 2004) ("Where the general summary or description of the invention describes a feature of the invention . . . and criticizes other products . . . that lack that same feature, this operates as a clear disavowal of these other products . . . .").
[42] '959 Patent 1:63-65.
[43] '959 Patent 7:31-42; 9:18-30.
[44] '959 Patent 1:66-2:1 ("However, a significant problem with source erase of flash EPROM cells is source diode leakage to the substrate during erasure."); 2:13-15 ("Band to band leakage wastes power since some of the diode current is dissipated in the substrate during erasure.").
[45] '959 Patent 9:36-37.
[46] *Praxair, Inc. v. ATMI, Inc.*, 543 F.3d 1306, 1324 (Fed. Cir. 2008).
[47] *Epistar Corp. v. Int'l Trade Comm'n*, 566 F.3d 1321 (Fed. Cir. 2009).
[48] *See SciMed*, 242 F.3d at 1342.

source leakage during source erase is critical to the invention.[49] Even Dr. Liu, in his declaration, noted that the '959 patent "addresses the issue of reducing source leakage during erasure of the source of a semiconductor device."[50] Reading the claim in light of the specification, a person of ordinary skill in the art would clearly understand that the invention refers to source erase, not to other types of erase procedures. Thus, the Court construes "source leakage" as: "leakage from the source terminal to the substrate terminal that occurs during source erase."

Claim Language	**Fast Memory's Proposed Construction**	**Defendants' Proposed Construction**
"a first doped region disposed under the edge of the stacked gate"	a part of the doped source region located beneath the edge of the stacked gate	the part of the doped source region located directly under the edge of the stacked gate

The parties agree that the first doped region must be near the edge of the stacked gate, in order to effectively redirect the current away from the damaged area. This dispute concerns whether the first doped region must be located directly under the edge of the stacked gate, or merely under it. Fast Memory argues that the gouge caused by the SAS etch removes silicon on the substrate and makes it impossible for the source side substrate to be directly under the edge of the stacked gate.

Expert testimony does not resolve the technical question of whether the SAS etch gouge prevents the first doped region from being located directly under the edge of the stacked gate. In his deposition, Dr. Liu stated that the etch may remove the silicon from the edge of the stacked gate and that the doped source region will be lower than "directly under the stack[ed] gate etch."[51] Dr. Liu concluded that locating the source region directly under the stacked gate would

[49] *Cf. Epistar*, 566 F.3d at 1337 ("Epistar also would limit "substrate" to a single layer. Although Epistar urges this court to apply the ALJ's construction, which was modified by the Commission, Epistar does not point to any intrinsic evidence to justify this limitation on the broad term "substrate." The Commission correctly declined to limit "substrate" to the preferred embodiments in the specification.").
[50] *See* Dkt. No. 130, Ex. G (Liu Decl.) at ¶ 18.
[51] Pl.'s App. at 431 (Liu Dep. 94:15-24).

render the patented invention unworkable.[52] Defendants' expert, Dr. Taylor, states that the first doped region must be located directly under the stacked gate edge, because locating the first doped region away from the surface of the source exponentially diminishes the strength of the electric field, thereby reducing the ability of the doped regions to redirect the erase current.[53] However, Dr. Taylor does not address whether the SAS gouge prevents the first doped region from being located directly under the edge of the stacked gate.

Fast Memory contends that the claim language provides for all possible locations of the first doped region. In response, Defendants cite to a preferred embodiment, which states that the first doped region is located "directly under the edge of the stacked gate."[54] Yet, the specification also describes the implanted source region as disposed "under the edge of the stacked gate."[55] Neither do the figures in the patent conclusively show that the first doped region must be located directly under the edge of the stacked gate.[56] The mixed evidence in the record does not show that the "character of the invention requires the limitation be a part of every embodiment," and the Court declines to import the "directly under" limitation urged by the Defendants into the claim.[57] The Court construes "a first doped region disposed under the edge of the stacked gate" as: "a part of the doped source region located beneath the edge of the stacked gate."

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[52] Dkt. No. 130, Ex. G (Liu Decl.) at ¶ 19 ("One of ordinary skill in the art would know that the first doped source region cannot be directly under the edge of the stacked gate. . . . In fact, were such a placement possible, placing the first doped source region immediately under the edge of the stacked gate would negate the benefits of the claimed invention. . . . As a result of the gouging process described above, the source side substrate is lowered to an area not directly underneath the gate. This in turn lowers the location of the first doped source region to an area that is not immediately underneath the gate.").

[53] D's App. at 415, 419 (Taylor Decl. ¶¶ 16, 23).

[54] '959 Patent 8:55-58. *See also* '959 Patent 9:41-43 (noting that the source regions are adjacent to the stacked gate). *But see* '959 Patent 8:48-51 ("The first source implant region and the second source implant region are located below the spacer and the edge of the stacked gate") (internal citations omitted).

[55] '959 Patent 3:48-52; 4:5-9; 4:40-44.

[56] Plaintiff contends that Figure 14B is incorrectly labeled and imprecisely drawn, since it does not show the SAS gouge.

[57] *Alloc*, 342 F.3d at 1370.

Claim Language	Fast Memory's Proposed Construction	Defendants' Proposed Construction
"a second doped region disposed at the edge of the doped source region under the stacked gate"	a part of the doped source region located next to the edge of the doped source region under the stacked gate	the part of the doped source region located directly under the stacked gate at the edge of the doped source region

Again, the parties dispute whether the second doped region must be located directly under the stacked gate. The specification does not use the phrase "directly under" with respect to the second doped region. Figures 8 and 14B show the second doped region further from the edge of the stacked gate than is the first doped region. Defendants' proposed construction varies from the claim language, which identifies a region rather than a fixed point. Therefore, the Court will not construe the second doped region as requiring it to be "directly under" the stacked gate edge. The Court construes "a second doped region disposed at the edge of the doped source region under the stacked gate" as: "a part of the doped source region located next to the edge of the doped source region under the stacked gate."

Claim Language	Fast Memory's Proposed Construction	Defendants' Proposed Construction
"dopant"	an impurity added to a semiconductor material	an impurity element added to a semiconductor to induce either electron conduction or hole conduction; a dopant is either N-type or P-type
"concentration of dopant"	This phrase does not require construction. In the alternative only, construe as: "an approximation of the amount of dopant per cubic centimeter"	the number of atoms of dopant per cubic centimeter (cm^3) of the semiconductor
wherein the second doped region has a higher concentration of dopant than the first doped region	This phrase does not require construction. In the alternative only, construe as: "the second doped region has a higher concentration of dopant per cubic centimeter than the first doped region"	wherein the second doped region has a higher concentration of the dopant type used to form the doped source region than the first doped region

There are two issues with respect to the construction of "dopant." The parties dispute (1) whether a dopant must be an element; and (2) whether a dopant must be either N-type or P-type. A dopant is an impurity introduced into the lattice of a semiconductor substrate in order to change the electrical conductivity of the semiconductor.[58] An N-type dopant induces electron conduction, "because each dopant atom has an 'extra' electron that is easily excited into a conductive state."[59] A P-type dopant induces hole conduction; as the hole accepts electrons from neighboring silicon atoms, the silicon becomes positively charged.[60]

The parties agree that a dopant may be an element. The Court only addresses the narrow question of whether a dopant may also be a compound, which consists of two or more different elements.[61] Fast Memory notes that dopants are often pure elements, such as phosphorous or boron, but contends that a dopant may also be a compound. The specification states that the preferred implant is the element phosphorous.[62] While the specification does not discuss the possibility of using a compound as a dopant, neither does it limit dopants to elements.

The parties' experts dispute whether a dopant must be a pure element. Fast Memory cites Dr. Liu's statement that the compound BF_2 (boron diflouride) was a known dopant in 1999, when the '959 patent was filed.[63] Defendants point to the *Academic Press Dictionary of Science and Technology*, published in 1992, which defines doping as the "addition of an impurity element."[64] Defendants' expert, Dr. Taylor, states that if BF_2 were injected into the silicon substrate, the compound would break up, leaving only free boron atoms to fall into the lattice of the silicon

[58] D's App. at 424 (Taylor Decl. ¶ 37).
[59] *Id.* at 425 (Taylor Decl. ¶ 39).
[60] *Id*.
[61] *See* Dkt. No. 130, Ex. G (Liu Decl.) at ¶ 7.
[62] '959 Patent 6:55-58; 7:66-67; Cl. 11, 16.
[63] Dkt. No. 130, Ex. G (Liu Decl.) at ¶ 7.
[64] D's App. at 498.

substrate.[65] The expert testimony is cursory and does not establish whether a dopant must be a pure element. The Court declines to confine the claim to its preferred embodiment, finds that a dopant must be an impurity added to a semiconductor, and does not exclude compounds of elements.

The second issue is whether a dopant must be either N-type or P-type. The specification discusses only dopants that are N-type or P-type,[66] but Fast Memory asserts that while most dopants are N-type or P-type, they can also be neutral. However, the weight of the evidence suggests that a dopant must be either N-type or P-type.[67] Even Dr. Liu states that dopants are either N-type or P-type,[68] although he notes that "dopants can be used to create neutral substrates that have no electrical conductivity."[69] Fast Memory did not show that neutral doping could accomplish the objectives of the '959 patent. The Court construes "dopant" as: "an impurity added to a semiconductor to induce either electron conduction or hole conduction; a dopant is either N-type or P-type."

The court will construe "concentration of dopant," since it does not have a plain and ordinary meaning.[70] Fast Memory contends that the actual number of atoms of dopant implanted into the semiconductor substrate cannot be determined, as the levels are measured in parts per trillion, and even the most accurate technology can only measure to the nearest 10 billion atoms

[65] D's App. at 425 (Taylor Decl. ¶ 38).
[66] '959 Patent 5:60-61; 6:42-48; 8:36-37; 9:38-40.
[67] *See* D's App. at 498 (Academic Press Dictionary of Science and Technology) ("Doping: (Electronics) The addition of an impurity element . . . to form P- or N-type material . . . ."); D's App. at 491 (Comprehensive Dictionary of Electrical Engineering) ("doping: the process of introducing impurity atoms into pure silicon to change its electrical properties. The impurities may be n-type . . . or p-type."); D's App. at 423-427 (Taylor Decl. ¶¶ 35-42) (explaining that it is well known to one skilled in the art that a dopant is either N-type or P-type); D's App. at 860 (Ratman Dep. 482:21-483:8) ("So it's only the N-type or P-type that's used.").
[68] *See* Dkt. No. 130, Ex. G (Liu Decl.) at ¶ 7 ("This silicon layer . . . is highly doped with either an N-Type or P-Type material.").
[69] *See id.*
[70] *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2007) ("When the parties present a fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it.").

per cubic centimeter (cm^3).[71] Defendants point to the specification, which refers to atoms of dopant per cubic centimeter (cm^3) as the unit of measurement.[72] However, the specification does not state a precise number of atoms; instead there are several references to "about" the number of atoms or a range of atoms per cubic centimeter (cm^3).[73] The Court is not persuaded from the evidence before it that the actual number of atoms per cubic centimeter can be measured. The Court construes "concentration of dopant" as: "an approximation of the amount of dopant per cubic centimeter."

The final disputed phrase is "wherein the second doped region has a higher concentration of dopant than the first doped region." Defendants argue that this phrase requires construction, since there is a dispute as to whether the first and second regions must be created using the same type dopant. However, this phrase plainly involves a comparison in concentrations of dopant, not dopant types. The plain and ordinary language of the claim controls.[74]

VI. Conclusion

For the reasons stated above, the jury will be instructed in accordance with the Court's construction of certain terms in the '959 patent, as set out in this Memorandum Opinion.

SO ORDERED.

February 2, 2010.

BARBARA M. G. LYNN
UNITED STATES DISTRICT JUDGE
NORTHERN DISTRICT OF TEXAS

[71] *See* Dkt. No. 130, Ex. G (Liu Decl.) at ¶ 9.
[72] '959 Patent 3:54-57 ("second doped region has a dopant concentration of about $5x10^{19}$ atoms/cm^3 and the first doped region has a dopant concentration of about $1x10^{19}$ atoms/cm^3"); 4:18-21; 4:49-52; 7:10-14; 8:52-58.
[73] *See, e.g.*, '959 Patent 4:18-21; 4:49-52; 8:1-17 ("In one embodiment, the first source implant is preferably phosphorous at various dosages ranging from between about 10^{14} ions/cm^2 to about $5x10^{25}$ ions/cm^2 . . . .").
[74] *See N. Telecom Ltd. v. Samsung Elecs. Co.*, 215 F.3d 1281, 1295 (Fed. Cir. 2000).